Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – Nov/Dec – 2017**

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|  |  |  |  |
| **Code :** | **14EC2068** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VHDL** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Observe the following declarative part in the architecture of a half adder     component XOR2    port (X,Y:inBIT;z: out BIT);    end component    component AND2    port (L,M:inBIT;z:out BIT);    end component what kind of architecture modeling is it ? Design Half adder circuit using the same type of modeling. | CO1 | 8 |
| b. | Show and explain a typical design flow process for designing VLSI circuits. | CO1 | 12 |
| (OR) | | | | |
| 2. | a. | What are the different types of architecture modeling? Mention the difference between all the models and write Entity of the following Block diagram  Y  Z  Combinational  Block  A  B  C | CO2 | 6 |
| b. | Explain Various VHDL data types. | CO1 | 14 |
|  |  |  |  |  |
| 3. | a. | Use VHDL conditional signal assignment statement and design 4X1 Multiplexer. | CO2 | 7 |
|  | b. | What are the differences that exist between Signal assignment and variable assignment? | CO1 | 3 |
|  | c. | Design the following circuit using VHDL structural model.  Related image | CO2 | 10 |
| (OR) | | | | |
| 4. |  | Develop a traffic light controller using VHDL. | CO3 | 20 |
|  |  |  |  |  |
| 5. | a. | Design 4 bit updown counter using VHDL. | CO2 | 10 |
|  | b. | Briefly discuss various delay models in VHDL. | CO1 | 10 |
| (OR) | | | | |
| 6. | a. | Develop a full adder VHDL test bench. | CO3 | 10 |
|  | b. | Design SISO Shift register using VHDL. | CO2 | 10 |
|  |  |  |  |  |
| 7. | a. | TYPE count is RANGE 0 TO 127;  TYPE states IS (idle, decision,read,write);  TYPE word IS ARRAY(15 DOWNTO 0) OF bit;  count'left = ---------- states'left = -------- word'left = ----------  count'right = ---------- states'right = ------- word'right = ----------  count'high = ---------- states'high = --------- word'high = ----------  count'low = ---------- states'low = ---------- word'low =----------  count'length = ---------- states'length = -------- word'length = --------- | CO1 | 8 |
|  | b. | Design JK and D flip flop | CO2 | 12 |
| (OR) | | | | |
| 8. |  | From the given information develop ALU usingVHDL program.  **ALU**  **ARITHMETIC**  **LOGICAL**  L  M  LSEL  A  B  A SEL  AOUT  LOUT   |  |  |  |  | | --- | --- | --- | --- | | **ASEL** | **AOUT** | **LSEL** | **LOUT** | | ADD | A+B | OR1 | L OR M | | SUB | A-B | AND1 | L AND M | | MUL | A\*B | NAND1 | L NAND M | | DIV | A/B | NOR1 | L NOR M | | AMIX | (A+B)\*(A-B) | EXOR1 | L XOR M | | BMIX | (A\*B)+A | LMIX | (L OR M) AND L | | CO3 | 20 |
|  | |  |  |  |
|  | | **Compulsory**: |  |  |
| 9. | a. | Compare function and procedure in sub program. | CO1 | 2 |
|  | b. | Write the syntax of package and package body and develop a VHDL package for Encoder circuit. | CO2 | 15 |
|  | c. | With one example Show how the generics are used in VHDL program. | CO1 | 3 |

ALL THE BEST